AMENDMENTS TO THE SPECIFICATION

Please amend the second full paragraph on page 2 as follows:

A sample hold circuit according to the invention includes a first switching element receiving an input potential of one of its electrodes, and being turned on for a first period; a second switching element connected at one of its electrodes to the other electrode of the first switching element, and being on for a second period; a first capacitor connected at one of its electrodes to the other electrode of the ~~first~~ second switching element, and receiving on the other electrode a predetermined potential; and a drive circuit having an input node connected to the other electrode of the second switching element and an output node connected to the other electrode of the first switching element, and providing a potential corresponding to a potential of the input node to the output node. Therefore, even when the input potential changes after the input potential is sampled by turning on the first and second switching elements for the first and second periods, respectively, the drive circuit holds the potential of the other electrode of the first switching element so that changes in the sampled potential can be suppressed.

Please amend the second paragraph on page 12 as follows:

Capacitor 29 is connected between output node N22 of level shift circuit 21 and output node N27 of level shift circuit 25. Capacitor [[26]] 29 transmits potential changes of node N22 to node N27, and transmits potential changes of node N27 to node N27.

Please amend the third paragraph on page 12 as follows:

Pull-up circuit 30 includes an N-type transistor 31 and a P-type transistor 32 connected in series between a node of a sixth power supply potential V6 of 15 V and output node N30. Output node N30 is connected to a load capacitance (parasitic capacitances of liquid crystal cell 2 and switches 15 and 16) 36. A gate of N-type transistor 31 receives output potential V22 of level shift circuit 21. A gate of P-type transistor 32 is connected to its drain. P-type transistor [[30]] 32 forms a diode element. Since sixth power supply potential V6 is set to operate N-type transistor 31 in a saturation region, N-type transistor 31 performs a so-called source-follower operation.

Please amend the third full paragraph on page 14 as follows:

When potential V22 of node N22 rapidly lowers, the capacity coupling performed through capacitor [[26]] 29 rapidly lowers potential V27 of node N27 by (VH - VL). In accordance with this, potential VO of output node N30 rapidly falls from VH to VL.

Please amend the first paragraph on page 17 as follows:

A drive circuit 42 in Fig. 9 is substantially the same as drive circuit [[37]] 41 in Fig. 8 except for that capacitor 29 is eliminated. If load capacitance 36 has a relatively small capacitance value, the sizes of transistors 24, 26, 31 and 35 can be reduced, and the parasitic capacitances of nodes N22 and N27 can be reduced. Therefore, potentials V22 and V27 of nodes N22 and N27 can be raised and lowered by the charging and discharging performed through resistance elements 22 and 28, although capacitor 29 is eliminated. In this modification, since

capacitor 2 is eliminated, the area occupied by the circuit can be further reduced.

Please amend the first full paragraph on page 20 as follows:

For example, when drive circuit 20 shown in Fig. 4 charges or discharges load capacitance 36, each of transistors 31, 32, 34 and 35 performs a so-called source-follower operation. In this operation, as output potential VO approaches input potential VI, a gate-source voltage of each of transistors 31, 32, 34 and 35 decreases, and the current drive capabilities of transistors 31, 32, 34 and 35 lower. Although lowering of the drive capabilities of transistors 32 and 34 can be prevented by increasing the gate electrode widths thereof, the increase in gate electrode width of transistors 31 and 35 results in increase in gate capacitance thereof, and thus lowers the operation speed of drive circuit 20. A ~~seventh~~ third embodiment overcomes this problem.

Please amend the first paragraph on page 22 as follows:

Raised potential V27 falls to (VI - VTN - |VTP|) because a current flows from node N27 to the line of fifth power supply potential V5 through N-type transistor 70. However, N-type transistor 70 is configured to have a small current drive capability for low power consumption. Therefore, a time required for lowering potential V27 of node N27 to the original level of (VI - VTN - |VTP|) is longer than a time required for raising potential [[V22]] V27 to the same level (VI - VTN - |VTP|).

Please amend the third full paragraph on page 23 as follows:

Lowered potential V27 falls to (VI - VTN - |VTP|) owing to a current flowing from node N27 to the line of fifth power supply potential [[VO]] V5 through N-type transistor 70. However, N-type transistor 70 is configured to have a small current drive capability for low power consumption. Therefore, a time required for lowering potential V27 of node N27 to the original level of (VI - VTN - |VTP|) is longer than a time required for raising potential [[V22]] V27 to the same level of (VI - VTN - |VTP

Please amend the first paragraph on page 26 as follows:

A drive circuit 90 in Fig. 24 is substantially the same as drive circuit 80 in Fig. 20 except for that signal ϕP is applied to the source of P-type transistor 24 instead of ground potential GND, and signal $/\phi P$ is applied to the drain of N-type transistor 26 instead of fourth power supply potential [[VO]] V4. In this modification, when P-type transistor 81 is on, the drain of P-type transistor 24 attains the "H" level so that flowing of a through-current through transistors 81, 23 and 24 can be prevented. Also, when N-type transistor 82 is on, the drain of N-type transistor 26 attains the "L" level so that flowing of a through-current through transistors 26, 27 and 82 can be prevented. Accordingly, current consumption of circuits 61 and 63 can be reduced.

Please amend the first paragraph on page 29 as follows:

This sixth embodiment can achieve the same effect as the fifth embodiment, and further can reduce the current consumption because it is possible to reduce the current flowing from the line of third power supply potential V3 to ground potential GND through transistors 97, 99, 100

and 98 as well as the current flowing from the line of fourth power supply potential [[VO]] V4 to the line of fifth power supply potential V5 through transistors 103, 105, 106 and 104. Since transistors 97, 98, 100 and 103 - 105 are eliminated, an area occupied by the circuit can be small.

Please amend the third paragraph on page 34 as follows:

In the initial state, switches S1b - S3b are off, and switch S4b is on so that nodes N20b, N122b, N30b and N121 hold last potential VI'. When switches S1b and S2b are turned on at time t1, all potentials V20b, V122b, V30b and VO of nodes N20b, N122b, N30b and N121 become equal to input potential VI. Potential V27 of node N27 becomes equal to (VI - |VTP| - VTN). Although the absolute value |VTP'| of the threshold voltage of P-type transistor 35 is higher than the absolute value |VTP| of the threshold voltage of ~~V-type~~ P-type transistor 27 by VOFb, all potentials V20b, V122b, V30b and VO can become equal to potential VI. This is because output node N121 is charged by the charging circuit to the level of input potential VI, but is no longer discharged.

Please amend the second paragraph on page 37 as follows:

A drive circuit 135 with the offset-compensating function shown in Fig. 42 is substantially the same as drive circuit 85 ~~with the offset-compensating function~~ shown in Fig. 22 except for that drive circuit 135 additionally includes an offset-compensating circuit formed of capacitors 122a, 122b, 126a and 126b as well as switches S1a - S4a and S1b - S4b. In this modification, when signals /ϕP and ϕP attain the "L" and "H" levels to turn on transistors 81 and 82, respectively, transistors 86 and 87 are simultaneously turned off so that flowing of a through-

current is prevented, and current consumption can be small.

Please amend the second full paragraph on page 45 as follows:

Constant current supply 171 is connected between the node of fourth power supply potential V4 and output node N30. Pull-down circuit 33 includes P- and N-type transistors 35 and 34 connected in series between a node of seventh power supply potential V7 of -10V and output node N30. The gate of P-type transistor 35 receives output potential V27 of level shift circuit 63. The gate of N-type transistor 34 is connected to its drain. N-type transistor 34 forms a diode element. Since seventh power supply potential V7 is set to operate P-type transistor 35 in a saturation region, P-type transistor 35 performs a so-called source-follower operation. Constant current supply [[71]] 171 is configured to provide the current of a minimum value required for generating the threshold voltage in each of transistors 34 and 35.

Please amend the first full paragraph on page 54 as follows:

When scanning line 4 is set to the selected level of "H", switches 235 - 237 are turned on, and switches 238 and 239 are turned off. Thereby, N-type transistor 232 is diode-connected by switches 236 and 237, and gradation current IG at the level corresponding to an image signal flows from current supply 240 to the line of ground potential GND through data line 6, switch 235 and N-type transistor 232. In this operation, the gate of N-type transistor 232 is at the level corresponding to gradation current IG, and capacitor 233 is charged to carry a gate-source voltage of N-type transistor [[230]] 232.